WHAT IS CLAIMED IS:

1. A calculation circuit for the division of a fixed-point input signal, which comprises a sequence of digital data values having a width of n bits, by an adjustable division factor 2^a for generating a divided fixed-point output signal, the circuit comprising:

a signal input for receiving a data value sequence of the fixed-point input signal;

a first addition circuit for adding the digital data value input at the signal input to a data value stored in a register to form a digital first summation data value comprising a width of max (n, a+1) +1 bits;

a shift circuit for shifting the first summation data value by a data bits towards the right to output the max (n, a+1) $-a$+1 more significant data bits of the first summation data value;

a logic circuit for logically ANDing the a less significant data bits of the first summation data value with a logic combination data value, or logically ORing the a less significant data bits of the first summation data value with an inverted logical combination data value, depending on a sign of the first summation data value, and for outputting a logically combined data value for storage in the register;

a second addition circuit for adding the data value output by the shift circuit to a value one for eliminating the DC signal component to form a second summation data value, depending on a sign of the first summation data value; and

a signal output for outputting the sequence of the second summation data value as a divided fixed-point output signal.

2. The calculation circuit of claim 1, further comprising a sign identification circuit for identifying a sign of the first summation data value.

3. The calculation circuit of claim 1, wherein the logic combination data value is equal to the division factor reduced by the value one.

4. The calculation circuit of claim 1, wherein the logic circuit comprises an inverter for inverting the logic combination date value.

5. The calculation circuit of claim 1, wherein the logic circuit comprises an AND gate for logically ANDing the logic combination data value with the *a* less significant data bits of the first summation data value.

6. The calculation circuit of claim 5, wherein the logic circuit comprises an OR gate for logically ORing the inverted logic combination data value with the *a* less significant data bits of the first summation data value.

7. The calculation circuit of claim 6, wherein the logic circuit comprises a multiplexer, the multiplexer comprising:

a first input, which is connected to the output of the AND gate,

a second input, which is connected to the output of the OR gate,

an output, which is connected to the register, and

a control input, which is driven by a sign identification circuit.

8. The calculation circuit of claim 1, wherein the second addition circuit comprises:

an adder for adding the data value output by the shift circuit to the value one to form the second summation data value; and

a multiplexer, which, as a function of a control signal received from a sign identification circuit, switches through the data value or the second summation data value, generated by the second adder, to the signal output of the calculation circuit.

9. The calculation circuit of claim 8, wherein when a positive sign of the first summation data value is identified by the sign identification circuit, the multiplexer of the second addition circuit switches through the data value output by the shift circuit to the signal output of the calculation circuit, and when a negative sign of the first summation data value is identified by the sign identification circuit, the multiplexer of the second addition circuit switches through the second summation data value output by the adder to the signal output of the calculation circuit.

10. The calculation circuit of claim 1, wherein when a positive sign of the first summation data value is identified by a sign identification circuit, the multiplexer of the logic circuit switches through the output of an AND gate to the register, and when a

negative sign of the first summation data value is identified by the sign identification circuit, the multiplexer of the logic circuit switches through the output of an OR gate to the register.

11. The calculation circuit of claim 1, wherein the division factor is a power value with a base 2 and an exponent *a*.

12. The calculation circuit of claim 11, wherein the exponent *a* corresponds to the number of data bits shifted toward the right by the shift circuit.

13. A circuit comprising:

receiving means for receiving an *n*-bit fixed-point signal;

dividing means for dividing the *n*-bit fixed point signal by a division factor of 2^a for generating a divided fixed-point output signal; and

control means for controlling the dividing means to adjust the division factor to decrease a variance of the divided fixed-point output signal.

14. The circuit of claim 13, wherein the dividing means comprises:

a first adding means for adding a digital data value of the *n*-bit fixed-point input signal to a stored data value to form a digital first summation data value comprising a width of max (n, a+1) +1 bits;

shifting means for shifting the first summation data value by *a* data bits

towards the right to output the max (n, a+1) –a+1 more significant data bits of the first summation data value;

means for ANDing the a less significant data bits of the first summation data value with a logic combination data value and means for ORing the a less significant data bits of the first summation data value with an inverted logical combination data value, wherein a logically combined data value output from the ANDing means or ORing means is selected depending on a sign of the first summation data value;

storing means for storing the logically combined data value selected as the stored data value;

a second adding means for adding the data value output by the shift circuit to a value one for eliminating the DC signal component to form a second summation data value, depending on a sign of the first summation data value; and

output means for outputting the sequence of the second summation data value as a divided fixed-point output signal.

15. The circuit of claim 14, wherein the control means comprises identifying means for identifying a sign of the first summation data value.

16. The circuit of claim 15, wherein the control means further comprises:

first selecting means connected to the ouput of the ANDing means and ORing means for controllably selecting the logically combined data value output from either the ANDing means and ORing means, in response to a control signal from the identifying means; and

second selecting means, connected to the output means of the circuit, for selecting an output of the shifting means or an output of the second adding means, in response to a control signal from the identifying means.

17. The circuit of claim 14, wherein the logic combination data value is equal to the division factor reduced by the value one.

18. The circuit of claim 14, wherein the exponent a corresponds to the number of data bits a shifted toward the right by the shift circuit.

19. A method for dividing a fixed-point input signal, which comprises a sequence of digital data values having a width of n bits, by an adjustable division factor 2^a for generating a divided fixed-point output signal, the method comprising the steps of:

receiving a data value sequence of the fixed-point input signal;

adding the digital data value of the fixed-point input signal to a stored data value to form a digital first summation data value comprising a width of max (n, a+1) +1 bits;

shifting the first summation data value by a data bits towards the right to generate the max (n, a+1) $-a$+1 more significant data bits of the first summation data value;

logically ANDing the a less significant data bits of the first summation data value with a logic combination data value, or logically ORing the a less significant data bits of the first summation data value with an inverted logical combination data value,

depending on a sign of the first summation data value, to generate a logically combined data value;

adding a value one to the shifted first summation data value for eliminating the DC signal component to form a second summation data value, depending on a sign of the first summation data value; and

outputting the sequence of the second summation data value as a divided fixed-point output signal.